A DIGITALLY CONTROLLED TONE & VOLUME CIRCUIT FOR AUTOSOUND SYSTEMS

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Abstract

A microprocessor controlled tone and volume circuit for automotive applications has been integrated in a CMOS technology. Very few external components are required while a high level of performance is achieved. Stereo source selection, volume, tone, loudness, balance and fader functions are provided.

Introduction

Design of audio control circuitry for automotive radios differs in several respects from audio controls in hi-fi. First, there are four speakers to be controlled independently.

Second, the supply voltage is relatively low (8-10V). As a consequence, noise must be kept to an absolute minimum to preserve dynamic range. Noise reduction systems further accentuate this by increasing the dynamic range of the system.

Finally, board space in a radio is very limited. Interface to the microprocessor must be simple and external components must be kept small in both number and physical size.

Description

As the block diagram of the IC illustrated in Figure 1 shows, the signal path consists of an input selector which is AC coupled to the tone control circuitry providing the bass and treble functions. Included is an internal op amp which drives a master stereo volume control with an 80 dB range and 2 dB resolution. An emitter follower then buffers the output of the volume control for driving the two speaker attenuators. These independently controlled attenuators with 40 dB range provide the balance and fader functions. Finally, another emitter follower couples the speaker attenuators to the outputs for driving the external power amplifiers.

This combination allows all front panel functions to be digitally controlled, simplifying chassis layout and assembly by eliminating the analog control lines. In addition, remote operation is now easily made possible.

Design Considerations

In order to achieve a high level of performance with respect to noise and THD, a combination of techniques were used. The amount of active circuitry is minimized in order to reduce noise. As a result, the signal path includes only one op amp in the tone circuit and uses emitter followers as buffers. Similarly, biasing for the signal path is kept simple and low impedance.

Using CMOS technology, excellent switches are available for implementing a potentiometer. A series of thin film resistors with CMOS switches at the taps replace a typical pot as shown in Figure 2. The silicon-chromium resistors employed have excellent linearity and matching characteristics and are used thoughout the design. Further, the high resistivity makes large value resistors practical.

Typical discrete CMOS switches can exhibit abnormalities such as clicks and pops when switching. This is a result of capacitive feedthough of the switching signal to the output, or DC shifts in the output level. Though careful design this can be eliminated by matching geometries to maintain charge balance. In addition, the load seen by the switches is high impedance compared to the channel resistance, causing no significant current to flow though them further reducing pops.

In this passive configuration the only noise source is the thermal noise of the channel impedance of the switches which can be made quite low.

Manuscript received June 9, 1986.

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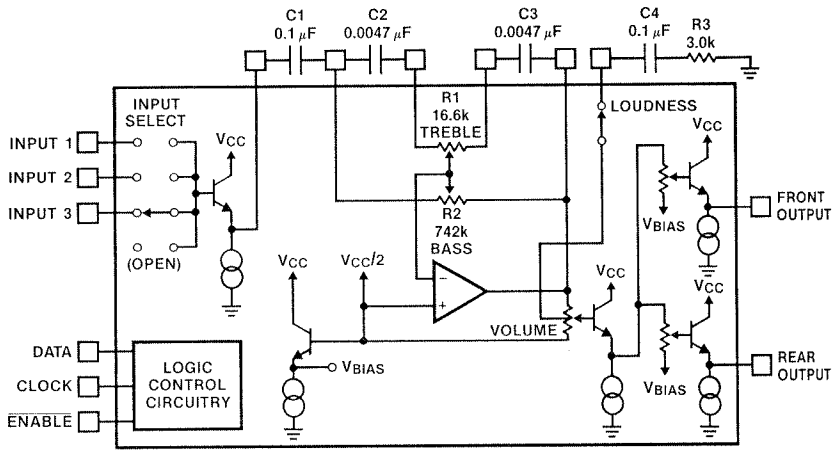

Figure 1. Internal architecture of audio processor (one channel).

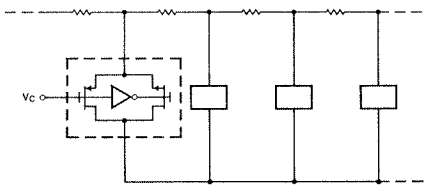

Figure 2. CMOS switched attenuator.

Input Switch

The input select circuit consists of a set of CMOS switches to select one of three possible direct coupled signal sources to an emitter follower buffer. Since the sources in automotive systems are operated from a single supply and thus have a DC component on their outputs, this configuration eliminates the need for individual coupling caps. The only coupling capacitor required couples the selector switch output to the tone control circuit.

The state of the switch in Figure 3 is determined by the control voltage Vc. When this line goes low, the PMOS device M2, and the NMOS device M1 both turn on, allowing the audio signal to pass to the emitter follower. To produce lower distortion, M3 also conducts, tying the bulk of the N channel devices to the source of M1, thereby eliminating body effect.

The input select circuit was designed such that expansion of the system is easily accomplished. Since the output of the selector switch is an emitter follower, it can be diode connected to another emitter follower in an auxiliary circuit if additional sources are required. In this configuration, the input select switch should be in the 'open' position and power to the auxiliary circuit is applied. When other inputs are selected, the power to the auxiliary circuit must be removed to prevent crosstalk.

Since the selector's output together with the input to the tone control circuitry are both made available, additional audio processing can easily be added such as noise reduction and/or equalization. Again AC coupling is required to the tone control input pin for proper operation.

The emitter follower on the selector switch output is biased at 1mA so it can drive a 3K ohm load with a 300 mV signal at less than 0.1% THD.

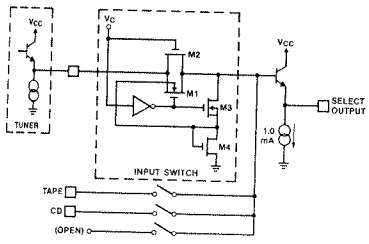

Figure 3. Input select circuitry.

The potentiometers R1 and R2 are again composed of a series of thin film resistors and switches with taps at 2 dB increments. This configuration gives a 12 dB range of boost and cut for both bass and treble functions.

The frequency response contours of the bass and treble functions are shown in Figure 5 for each step of equal amount of boost and cut applied. By changing the external capacitors from their original values the frequency response curves can together be shifted up or down the frequency spectrum if desired.

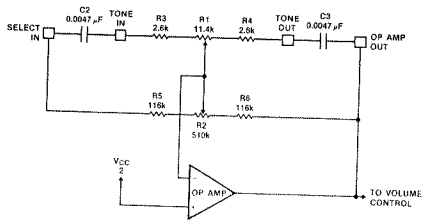

Figure 4. Simplified tone control.

Tone Control

Figure 4 shows the configuration used to implement the bass and treble control functions. It is a typical inverting amplifier with R1 controlling the high frequency response while R2 controls the response at low frequencies. With this configuration a shelving type of equalization is performed with the turnover frequencies dependent upon the external capacitors C2 and C3. Since the ratio of these capacitors determines the mid frequency gain, they should both be equal for symmetric tone response [C1=C2=C]. The lower turnover frequency is determined by the external capacitors together with the sum of R5 plus R2 [Fl=1/sC(R5+R2)], while R3 and the external capacitors set the upper turnover frequency [Fh=1/sCR3].

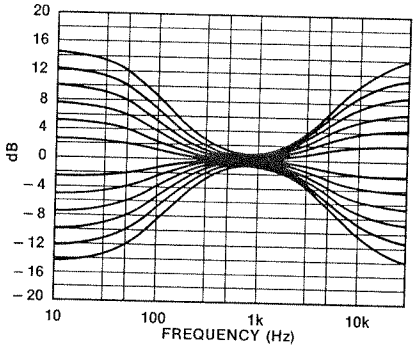

Figure 5. Tone response contours.

Low Noise Devices

For a passive CMOS switch, thermal noise resulting from the channel impedance is important. To realize an op amp the 1/F noise becomes important. Here a low noise op amp was developed using a unique input structure.

Since the op amp can be a major contributor to the overall output noise of the IC, its design was critical. Several different structures were evaluated for use in the op amp input stage. Of these the lateral NPN inherent in CMOS was found to be the lowest noise, and exhibit almost no 1/F low frequency noise as shown in Figure 6. Also it was discovered that the noise of the P channels could be reduced by approximately five times. This is accomplished by not implanting charge into their gate regions as is normally done to lower the threshold voltage to match that of the N channel devices.

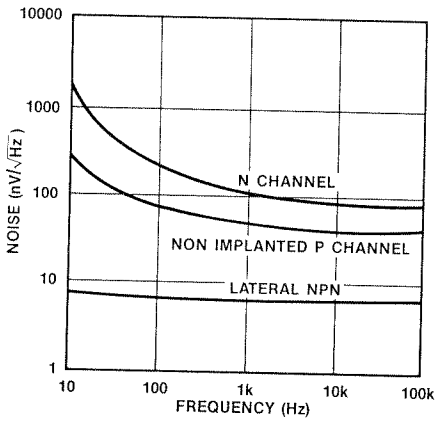

Figure 6. CCIR weighted noise of transistors.

The structure of the lateral NPN in CMOS is formed, as shown in Figure 7, within a P- well with a P+ guard ring which becomes the base. In the center of the P- well is an N+ diffusion working as the emitter, while between this and the base diffusion is a surrounding N+ ring acting as the collector. Also formed is a parasitic vertical NPN transistor between the emitter and substrate plus a N channel MOSFET between the lateral collector and emitter which is turned off by tying its gate to the emitter.

The current leaving the emitter is thus the sum of the vertical and lateral collector currents. The vertical current turns out to be approximately three times the lateral current but is not well controlled, while the lateral beta is around 300.

The vertical NPN has a similar structure and is built without the lateral collector ring. The beta on this device is typically 1000.

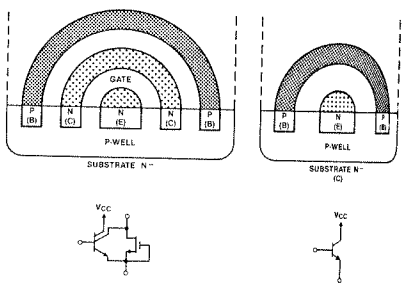

Figure 7. BJT structures in CMOS.

Op Amp Design

The internal structure of the op amp is a classical two stage design using the lateral NPN's as input devices Q1 and Q2 as shown in Figure 8. The non-implanted P channel devices M7 and M8 serve as active loads to the first stage converting the differential signal to single ended for the second stage M9 and M10. This stage drives the class A output stage consisting of a vertical NPN (Q4) and its current source M11.

The biasing of the op amp is developed from the current flowing though the 17K ohm resistor originating from an internal regulator. This directly sets the currents in the second and output stages. In addition, a current is mirrored into the lateral collector of Q3. The emitter current (which also includes vertical current) is then used to bias the input stage. This way any bias dependence upon the vertical to lateral collector split is canceled and the gain bandwidth product remains constant.

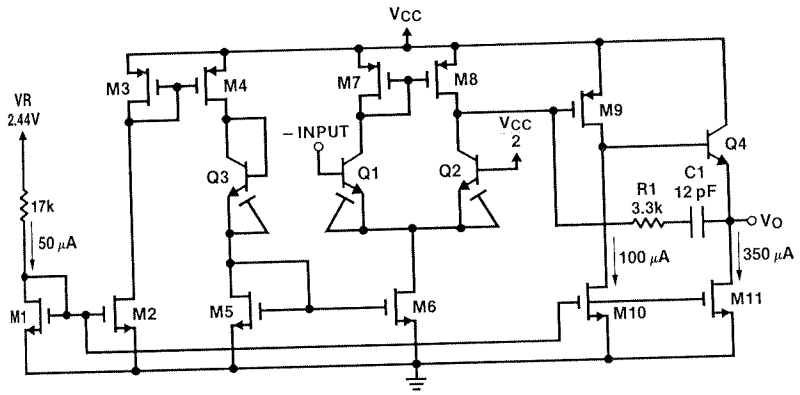

Figure 8. Internal architecture of the op amp.

Volume Attenuator

The volume function is accomplished by a two stage attenuator which is composed of a series of thin film resistors with CMOS switches at the taps as shown in Figure 9. To eliminate clicks and pops when changing attenuation levels, no significant DC current is allowed to flow though the CMOS switches and resistors. The same potential is developed at both ends of the resistor string by the bias circuitry since DC coupling is maintained from the output of the op amp.

The first attenuator is configured in 16 dB steps, while the second attenuator provides the fine 2 dB resolution, which when combined gives 80 dB of control range. The output of the second attenuator is then buffered by an emitter follower for driving the two speaker attenuators.

To perform the optional loudness function, external components (R3 and C4 in Figure 9) are used. When loudness is activated, the internal 3K resistor is replaced by a resistor and capacitor combination to give the added bass boost at low volume levels. Treble boost can also be added if desired by a resistor and capacitor in series from the op amp output to the loudness pin. To prevent pops when activating the loudness function, internal circuitry keeps capacitor C4 charged to half supply when loudness is off. Thus when loudness is activated, no current has to flow to charge up the capacitor.

Speaker Attenuators

The speaker attenuators are similar to that of the volume attenuator except that each output is individually controlled to provide the balance and fader functions. Again no DC voltage is imposed across the attenuator which minimize pops when changing levels. Here the first attenuator has 8 dB steps while the second has the fine 2 dB steps. Together they provide 40 dB of range. Their outputs are buffered by emitter followers running at 350 μA to drive the external power amplifiers.

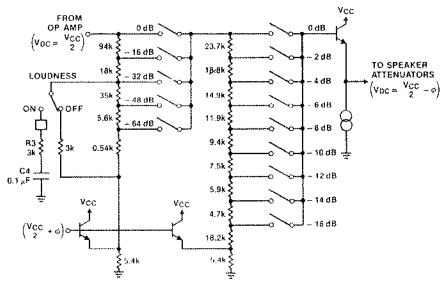

Figure 9. Volume attenuator detail.

A start up pulse is generated by Q11 and is used to reset the internal data registers. At initial turn on the device is reset to maximum attenuation in volume and speaker attenuators together with flat tone to mute any transients.

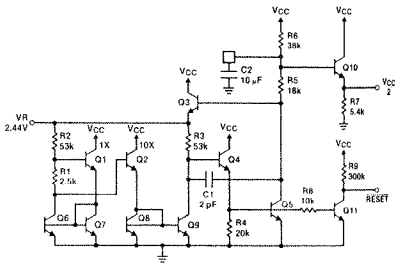

Figure 10. Delta VBE regulator.

Biasing

The biasing circuitry has three functions. First, to provide a low noise reference voltage which tracks supply for the op amp and attenuators. Second, it should provide a reference voltage independent of supply which sets the GBW of the op amp and finally, to furnish a reset signal on power up.

The biasing is accomplished by a delta VBE regulator employing lateral and vertical BJTs as shown in Figure 10. A reference current is imposed across R1 by a delta VBE developed by the vertical bipolar devices Q1 and Q2. The output voltage is generated by this reference current flowing though R2 plus the base-emitter voltage of Q1 and Q7. Lateral BJTs Q6-Q9 serve as current mirrors to keep Q1 and Q2 operating at the same currents.

To provide a low impedance half supply voltage to the op amp and attenuator circuits, Q10 is used. Since the voltage at the base of Q3 is held constant over supply variations, the decouple point at the base of Q10 will change with supply.

Data Communication.

The communication format for entering data ir the audio processor is a three wire MICROWIRE interface consisting of TTL compatible data, clock a enable lines. When the enable line goes high, data latched and executed.

The eleven bit data word as shown in Figure 1 broken up into three parts. The first, being the c select address, must be 1,0 in order to rec additional data. This allows sharing of the between the phase locked loops and a processor without additional decoding. The three bits are used to select the desired functic be controlled (ie: volume). The remaining six bits constitute data for that function. For eas programming, additional don't care bits ma inserted prior to the function address as t eventually are shifted out internally.

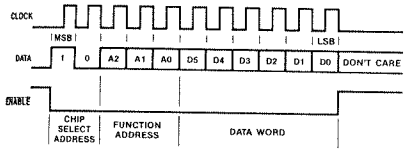

Figure 11. Data communications format.

System Organization

A completely microprocessor controlled automotive radio is shown in Figure 12, broken down into functional blocks. A master CPU controls the AM and FM tuners together with the audio processor on a serial bus. Front panel display and controls also interface directly to the CPU eliminating analog control lines, thus simplifying chassis layout and assembly.

Since the audio processor is reset upon power up, the CPU will have to send out data to return the IC to its previous state as is now normally done with the phase locked loops.

Three inputs plus noise reduction connect directly to the audio processor, while its outputs drive individual power amplifiers for each speaker. With nominal input levels of 300 mV RMS at maximum volume, a power amplifier with a gain of 40 dB provides enough overdrive for the speakers.

Performance

The graph in Figure 13 shows the 1Khz total harmonic distortion versus input signal level at three constant output levels which correspond to clipping levels at the speakers with different amplifier gains. With a 300 mV RMS signal at full output the THD is less than 0.1%, rising to only 0.13% as the input voltage reaches 1 Volt RMS. With lower output levels the THD drops significantly to less than 0.025% at all input levels.

The signal to noise ratio achieved when driving a power amplifier with 40 dB of gain and a power output of 6 Watts is typically greater than 80 dB as shown in Figure 14. The changing source impedance of the volume attenuator accounts for the variation in noise with attenuation.

When changing attenuation levels some pops are observed at the outputs. These occur as DC shifts in output level with no glitches and are typically less than 4 mV peak in amplitude lowering to less the 0.5 mV at most listening levels. A summary of performance is shown in Table 1.

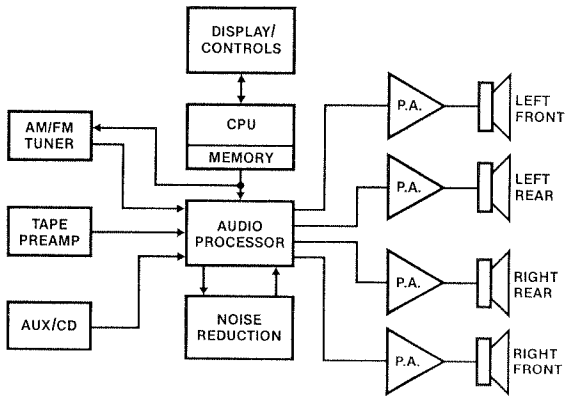

Figure 12. Digitally controlled automotive radio.

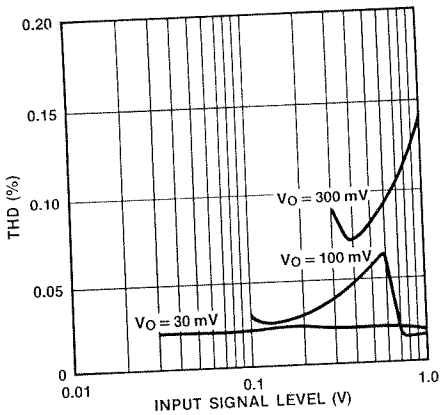

Figure 13. 1Khz THD versus input voltage.

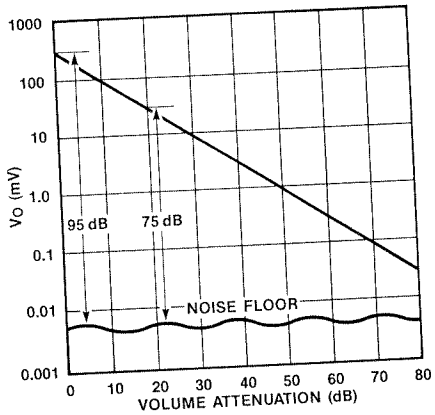

Figure 14. S/N versus attenuation.

Vsupply=10V, Bass and Treble Flat

Supply Current	20	mA
Max. Volume CCIR Noise	6.0	μV
Max. Volume 20-20 Khz Noise	5.0	μV
Min. Volume CCIR Noise	4.0	μV
Min. Volume 20-20 Khz Noise	3.5	μv
Dynamic Range	110	dB
Channel Separation	80	dB
Input Isolation	90	dB
Frequency Response Fh=-1dB	400	Khz
Attenuator Tracking	0.5	dB
Maximum Clock Frequency	500	Khz

Table 1. Performance Summary.

Conclusion

The microprocessor controlled audio sign processor as described is aimed specifically at th automotive marketplace. This IC includes all the fron panel audio control functions found in typical applications. Full digital control can now be easily realized in autosound systems.

References

(1) MICROWIRE is a trademark of National Semiconductor Corporation, Santa Clara, CA.

Acknowledgements

My thanks to Bill Jett and Don Sauer for their help and support in the development of this project.

Biography

Randy G. Flatness received a B.S. in Electroni Engineering from California Polytechnic State University in San Luis Obispo in 1982. Upon graduation he joined the product engineering group at National Semiconductor where he was involved with Bipolar and CMOS linear circuits. In 1984 he transfered to the Consumer Linear Design group at National Semiconductor where he is currently engaged in Bipolar and CMOS circuit design and development.